Freeform Search

Database: US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Term: multiply near4 add near7 enabl$3 near9 instruction$1

Display: 20 **Documents in Display Format:** TI **Starting with Number** 1

Generate: ○ **Hit List** ◉ **Hit Count** ○ **Side by Side** ○ **Image**

Search Clear Interrupt

Search History

DATE: Monday, March 01, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L7	multiply near4 add near7 enabl$3 near9 instruction$1	11	L7
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L6	multiply near4 add near7 enabl$3 near9 instruction$1	12	L6
DB=USPT; PLUR=YES; OP=OR			
L5	L4 not l2	58	L5
L4	pair$1 near5 instruction$1 and decod$3 near9 graphic$1	71	L4
L3	6308253.pn. and decod$3	1	L3
L2	pair$1 near5 instruction$1 and decod$3 near5 graphic$1	13	L2
L1	pair$1 near5 instruction$1 near6 (enabl$3 or activat$3) and decod$3 near5 graphic$1	0	L1

END OF SEARCH HISTORY

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 20 of 20 returned.

☐ 1. Document ID: US 6502115 B2

L10: Entry 1 of 20 File: USPT Dec 31, 2002

US-PAT-NO: 6502115
DOCUMENT-IDENTIFIER: US 6502115 B2
** See image for Certificate of Correction **

TITLE: Conversion between packed floating point data and packed 32-bit integer data in different architectural registers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 6480868 B2

L10: Entry 2 of 20 File: USPT Nov 12, 2002

US-PAT-NO: 6480868
DOCUMENT-IDENTIFIER: US 6480868 B2

TITLE: Conversion from packed floating point data to packed 8-bit integer data in different architectural registers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 6332186 B1

L10: Entry 3 of 20 File: USPT Dec 18, 2001

US-PAT-NO: 6332186
DOCUMENT-IDENTIFIER: US 6332186 B1

TITLE: Vector register addressing

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 4. Document ID: US 6304963 B1

L10: Entry 4 of 20 File: USPT Oct 16, 2001

h e b b g e e e f e ef b e

US-PAT-NO: 6304963
DOCUMENT-IDENTIFIER: US 6304963 B1

TITLE: Handling exceptions occuring during processing of vector instructions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 5. Document ID: US 6292815 B1

L10: Entry 5 of 20 File: USPT Sep 18, 2001

US-PAT-NO: 6292815
DOCUMENT-IDENTIFIER: US 6292815 B1
**** See image for Certificate of Correction ****

TITLE: Data conversion between floating point packed format and integer scalar format

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 6. Document ID: US 6282634 B1

L10: Entry 6 of 20 File: USPT Aug 28, 2001

US-PAT-NO: 6282634
DOCUMENT-IDENTIFIER: US 6282634 B1

TITLE: Apparatus and method for processing data having a mixed vector/scalar register file

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 7. Document ID: US 6266769 B1

L10: Entry 7 of 20 File: USPT Jul 24, 2001

US-PAT-NO: 6266769
DOCUMENT-IDENTIFIER: US 6266769 B1

TITLE: Conversion between packed floating point data and packed 32-bit integer data in different architectural registers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 8. Document ID: US 6263426 B1

L10: Entry 8 of 20 File: USPT Jul 17, 2001

US-PAT-NO: 6263426
DOCUMENT-IDENTIFIER: US 6263426 B1

h e b b g e e e f e ef b e

TITLE: Conversion from packed floating point data to packed 8-bit integer data in different architectural registers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 9. Document ID: US 6253312 B1

L10: Entry 9 of 20 File: USPT Jun 26, 2001

US-PAT-NO: 6253312
DOCUMENT-IDENTIFIER: US 6253312 B1

TITLE: Method and apparatus for double operand load

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 10. Document ID: US 6247116 B1

L10: Entry 10 of 20 File: USPT Jun 12, 2001

US-PAT-NO: 6247116
DOCUMENT-IDENTIFIER: US 6247116 B1
**** See image for Certificate of Correction ****

TITLE: Conversion from packed floating point data to packed 16-bit integer data in different architectural registers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 11. Document ID: US 6247113 B1

L10: Entry 11 of 20 File: USPT Jun 12, 2001

US-PAT-NO: 6247113
DOCUMENT-IDENTIFIER: US 6247113 B1

TITLE: Coprocessor opcode division by data type

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 12. Document ID: US 6189094 B1

L10: Entry 12 of 20 File: USPT Feb 13, 2001

US-PAT-NO: 6189094
DOCUMENT-IDENTIFIER: US 6189094 B1

TITLE: Recirculating register file

h e b b g e e e f e ef b e

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 13. Document ID: US 6170001 B1

L10: Entry 13 of 20 File: USPT Jan 2, 2001

US-PAT-NO: 6170001
DOCUMENT-IDENTIFIER: US 6170001 B1

TITLE: System for transfering format data from format register to memory wherein format data indicating the distribution of single or double precision data type in the register bank

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☑ 14. Document ID: US 6105129 A

L10: Entry 14 of 20 File: USPT Aug 15, 2000

US-PAT-NO: 6105129
DOCUMENT-IDENTIFIER: US 6105129 A
**** See image for Certificate of Correction ****

TITLE: Converting register data from a first format type to a second format type if a second type instruction consumes data produced by a first type instruction

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 15. Document ID: US 6094719 A

L10: Entry 15 of 20 File: USPT Jul 25, 2000

US-PAT-NO: 6094719
DOCUMENT-IDENTIFIER: US 6094719 A

TITLE: Reducing data dependent conflicts by converting single precision instructions into microinstructions using renamed phantom registers in a processor having double precision registers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 16. Document ID: US 5995122 A

L10: Entry 16 of 20 File: USPT Nov 30, 1999

US-PAT-NO: 5995122
DOCUMENT-IDENTIFIER: US 5995122 A

TITLE: Method and apparatus for parallel conversion of color values from a single precision floating point format to an integer format

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 17. Document ID: US 5884070 A

L10: Entry 17 of 20 File: USPT Mar 16, 1999

US-PAT-NO: 5884070
DOCUMENT-IDENTIFIER: US 5884070 A

TITLE: Method for processing single precision arithmetic operations in system where two single precision registers are aliased to one double precision register

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 18. Document ID: US 5673407 A

L10: Entry 18 of 20 File: USPT Sep 30, 1997

US-PAT-NO: 5673407
DOCUMENT-IDENTIFIER: US 5673407 A

TITLE: Data processor having capability to perform both floating point operations and memory access in response to a single instruction

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 19. Document ID: US 5487022 A

L10: Entry 19 of 20 File: USPT Jan 23, 1996

US-PAT-NO: 5487022
DOCUMENT-IDENTIFIER: US 5487022 A

TITLE: Normalization method for floating point numbers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 20. Document ID: US 5442760 A

L10: Entry 20 of 20 File: USPT Aug 15, 1995

US-PAT-NO: 5442760
DOCUMENT-IDENTIFIER: US 5442760 A

TITLE: Decoded instruction cache architecture with each instruction field in multiple-instruction cache line directly connected to specific functional unit

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b g e e e f e ef b e

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
SINGLE	1490256
SINGLES	1476
TWO	2559261
TWOES	0
TWOS	1908
TWOE	1
PRECISION$1	0
PRECISION	193486
PRECISIONE	11
PRECISIONS	903
PRECISION7	6
(SINGLE NEAR2 PRECISION$1 NEAR5 (TWO OR PAIR$1) NEAR7 INSTRUCTION$1 AND (GRAPHIC$3 OR IMAG$3)).USPT.	20

There are more results than shown above. Click here to view the entire set.

Display Format: TI Change Format

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Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 20 of 33 returned.

☐ 1. Document ID: US 6571328 B2

L1: Entry 1 of 33 File: USPT May 27, 2003

US-PAT-NO: 6571328
DOCUMENT-IDENTIFIER: US 6571328 B2

TITLE: Method and apparatus for obtaining a scalar value directly from a vector register

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 6530011 B1

L1: Entry 2 of 33 File: USPT Mar 4, 2003

US-PAT-NO: 6530011
DOCUMENT-IDENTIFIER: US 6530011 B1

TITLE: Method and apparatus for vector register with scalar values

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 6366998 B1

L1: Entry 3 of 33 File: USPT Apr 2, 2002

US-PAT-NO: 6366998
DOCUMENT-IDENTIFIER: US 6366998 B1
**** See image for Certificate of Correction ****

TITLE: Reconfigurable functional units for implementing a hybrid VLIW-SIMD programming model

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 4. Document ID: US 6332186 B1

L1: Entry 4 of 33 File: USPT Dec 18, 2001

h e b b g e e e f e g ef b e

US-PAT-NO: 6332186
DOCUMENT-IDENTIFIER: US 6332186 B1

TITLE: Vector register addressing

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 5. Document ID: US 6304963 B1

L1: Entry 5 of 33 File: USPT Oct 16, 2001

US-PAT-NO: 6304963
DOCUMENT-IDENTIFIER: US 6304963 B1

TITLE: Handling exceptions occuring during processing of vector instructions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 6. Document ID: US 6282634 B1

L1: Entry 6 of 33 File: USPT Aug 28, 2001

US-PAT-NO: 6282634
DOCUMENT-IDENTIFIER: US 6282634 B1

TITLE: Apparatus and method for processing data having a mixed vector/scalar register file

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 7. Document ID: US 6247113 B1

L1: Entry 7 of 33 File: USPT Jun 12, 2001

US-PAT-NO: 6247113
DOCUMENT-IDENTIFIER: US 6247113 B1

TITLE: Coprocessor opcode division by data type

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 8. Document ID: US 6189094 B1

L1: Entry 8 of 33 File: USPT Feb 13, 2001

US-PAT-NO: 6189094
DOCUMENT-IDENTIFIER: US 6189094 B1

TITLE: Recirculating register file

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Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 18 of 18 returned.

☐ 1. Document ID: US 20030163667 A1

Using default format because multiple data bases are involved.

L14: Entry 1 of 18 File: PGPB Aug 28, 2003

PGPUB-DOCUMENT-NUMBER: 20030163667
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030163667 A1

TITLE: Vector processing system

PUBLICATION-DATE: August 28, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Barlow, Stephen	Cambridge		GB	
Bailey, Neil	Cambridge		GB	
Ramsdale, Timothy	Cambridge		GB	
Plowman, David	Saffron Walden		GB	
Swann, Robert	Cambridge		GB	

US-CL-CURRENT: 712/7; 712/222

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20030154361 A1

L14: Entry 2 of 18 File: PGPB Aug 14, 2003

PGPUB-DOCUMENT-NUMBER: 20030154361
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030154361 A1

TITLE: Instruction execution in a processor

PUBLICATION-DATE: August 14, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Barlow, Stephen	Cambridge		GB	
Bailey, Neil	Cambridge		GB	

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Ramsdale, Timothy	Cambridge	GB
Plowman, David	Saffron Walden	GB
Swann, Robert	Cambridge	GB

US-CL-CURRENT: 712/214

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 3. Document ID: US 20020032848 A1

L14: Entry 3 of 18 File: PGPB Mar 14, 2002

PGPUB-DOCUMENT-NUMBER: 20020032848
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020032848 A1

TITLE: Method and apparatus for obtaining a scalar value directly from a vector register

PUBLICATION-DATE: March 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Liao, Yu-Chung C.	Austin	TX	US	
Sandon, Peter A.	Essex Junction	VT	US	
Cheng, Howard	Sammamish	WA	US	
Van Hook, Timothy J.	Atherton	CA	US	

US-CL-CURRENT: 712/4; 712/208, 712/222

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 4. Document ID: US 6571328 B2

L14: Entry 4 of 18 File: USPT May 27, 2003

US-PAT-NO: 6571328
DOCUMENT-IDENTIFIER: US 6571328 B2

TITLE: Method and apparatus for obtaining a scalar value directly from a vector register

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 5. Document ID: US 6530011 B1

L14: Entry 5 of 18 File: USPT Mar 4, 2003

US-PAT-NO: 6530011

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DOCUMENT-IDENTIFIER: US 6530011 B1

TITLE: Method and apparatus for vector register with scalar values

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 6. Document ID: US 6282634 B1

L14: Entry 6 of 18 File: USPT Aug 28, 2001

US-PAT-NO: 6282634
DOCUMENT-IDENTIFIER: US 6282634 B1

TITLE: Apparatus and method for processing data having a mixed vector/scalar register file

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 7. Document ID: US 6247113 B1

L14: Entry 7 of 18 File: USPT Jun 12, 2001

US-PAT-NO: 6247113
DOCUMENT-IDENTIFIER: US 6247113 B1

TITLE: Coprocessor opcode division by data type

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 8. Document ID: US 6189094 B1

L14: Entry 8 of 18 File: USPT Feb 13, 2001

US-PAT-NO: 6189094
DOCUMENT-IDENTIFIER: US 6189094 B1

TITLE: Recirculating register file

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 9. Document ID: US 6173366 B1

L14: Entry 9 of 18 File: USPT Jan 9, 2001

US-PAT-NO: 6173366
DOCUMENT-IDENTIFIER: US 6173366 B1
**** See image for Certificate of Correction ****

TITLE: Load and store instructions which perform unpacking and packing of data bits in separate vector and integer cache storage

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 10. Document ID: US 6154831 A

L14: Entry 10 of 18 File: USPT Nov 28, 2000

US-PAT-NO: 6154831
DOCUMENT-IDENTIFIER: US 6154831 A
** See image for Certificate of Correction **

TITLE: Decoding operands for multimedia applications instruction coded with less number of bits than combination of register slots and selectable specific values

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 11. Document ID: US 6141673 A

L14: Entry 11 of 18 File: USPT Oct 31, 2000

US-PAT-NO: 6141673
DOCUMENT-IDENTIFIER: US 6141673 A

TITLE: Microprocessor modified to perform inverse discrete cosine transform operations on a one-dimensional matrix of numbers within a minimal number of instructions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 12. Document ID: US 6061521 A

L14: Entry 12 of 18 File: USPT May 9, 2000

US-PAT-NO: 6061521
DOCUMENT-IDENTIFIER: US 6061521 A

TITLE: Computer having multimedia operations executable as two distinct sets of operations within a single instruction cycle

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 13. Document ID: US 6047372 A

L14: Entry 13 of 18 File: USPT Apr 4, 2000

US-PAT-NO: 6047372
DOCUMENT-IDENTIFIER: US 6047372 A
** See image for Certificate of Correction **

TITLE: Apparatus for routing one operand to an arithmetic logic unit from a fixed

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register slot and another operand from any register slot

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 14. Document ID: US 6009505 A

L14: Entry 14 of 18 File: USPT Dec 28, 1999

US-PAT-NO: 6009505
DOCUMENT-IDENTIFIER: US 6009505 A

TITLE: System and method for routing one operand to arithmetic logic units from fixed register slots and another operand from any register slot

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 15. Document ID: US 5717947 A

L14: Entry 15 of 18 File: USPT Feb 10, 1998

US-PAT-NO: 5717947
DOCUMENT-IDENTIFIER: US 5717947 A
** See image for Certificate of Correction **

TITLE: Data processing system and method thereof

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 16. Document ID: US 5717881 A

L14: Entry 16 of 18 File: USPT Feb 10, 1998

US-PAT-NO: 5717881
DOCUMENT-IDENTIFIER: US 5717881 A
** See image for Certificate of Correction **

TITLE: Data processing system for processing one and two parcel instructions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 17. Document ID: US 5423051 A

L14: Entry 17 of 18 File: USPT Jun 6, 1995

US-PAT-NO: 5423051
DOCUMENT-IDENTIFIER: US 5423051 A

TITLE: Execution unit with an integrated vector operation capability

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Drawi De

☐ 18. Document ID: US 4873630 A

L14: Entry 18 of 18 File: USPT Oct 10, 1989

US-PAT-NO: 4873630
DOCUMENT-IDENTIFIER: US 4873630 A

TITLE: Scientific processor to support a host processor referencing common memory

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Drawi De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
(10 AND 2).PGPB,USPT.	18
(L10 AND L2).PGPB,USPT.	18

Display Format: - Change Format

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Refine Search

Search Results -

Term	Documents
(10 AND 2).PGPB,USPT.	18
(L10 AND L2).PGPB,USPT.	18

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L14

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, March 03, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT; PLUR=YES; OP=OR			
L14	l10 and l2	18	L14
L13	l1 and l2	579	L13
L12	L11 and l10	19	L12
L11	l2 or l4 or l5 or l6 or l7 or l8 or l9	7234	L11
L10	l1 and (id$1 or identif$7 or address$5 or index$3) near5 scalar near8 vector$1	36	L10
L9	(712/2)![CCLS]	76	L9
L8	(708/524)[CCLS]	83	L8
L7	(708/495)[CCLS]	160	L7
L6	(708/501)[CCLS]	90	L6
L5	(708/523)[CCLS]	127	L5
L4	(708/523)![CCLS]	127	L4

h e b b cg b e e ch

L3	(708/224)![CCLS]	0	L3
L2	(712/3-222)![CCLS]	6877	L2
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L1	(single$1 or double$1) near5 (two or pair$1) near7 instruction$1	1501	L1

END OF SEARCH HISTORY